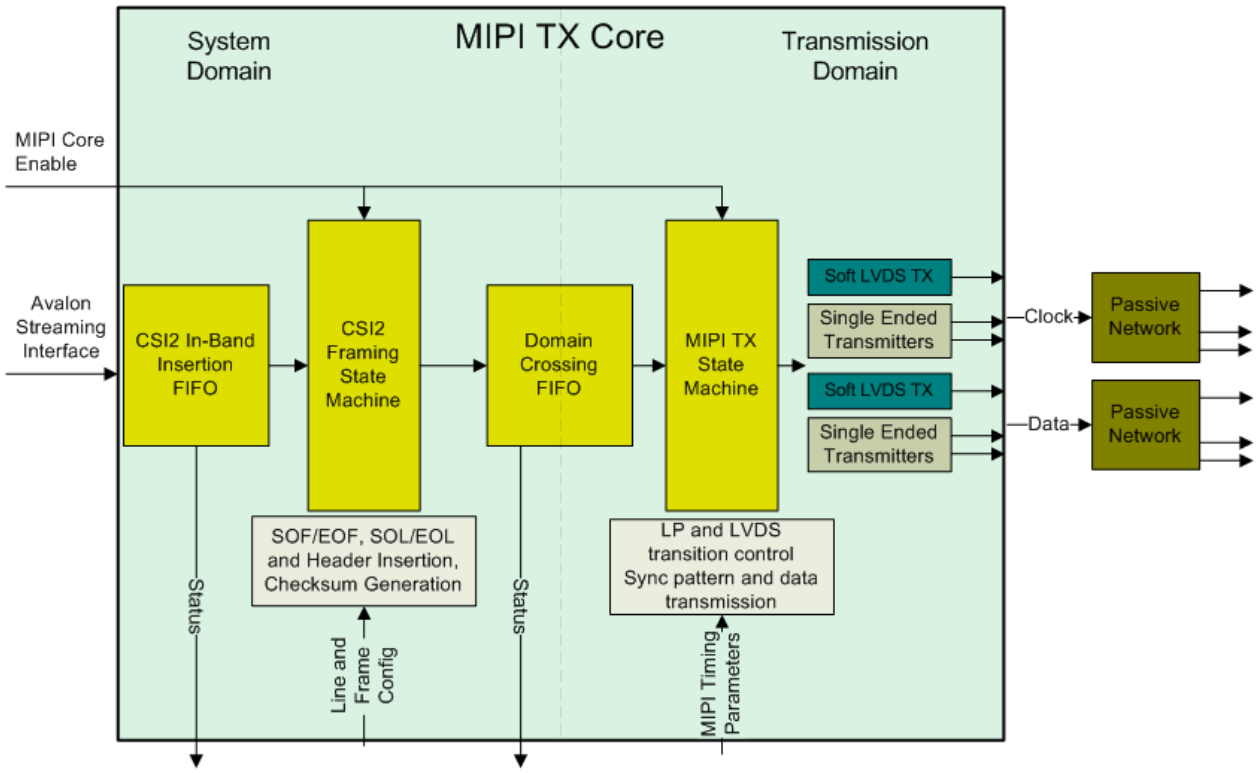
FORESYS

MIPI CSI2 Tx Core

Description

The Foresys MIPI Core provides a fast path to integrating Image Sensors into a wide variety of products based on Altera devices. It is designed to convert an internal payload agnostic Avalon Streaming data bus to MIPI/CSI2 data.



Base Features

- ✓ Provides Compatible MIPI D-Phy v1.1 physical layer using FPGA LVDS/LVCMOS IO and passive network
- ✓ Supports CSI-2 protocol for unidirectional data transfer
- ✓ Compatible with D-PHY Configured for 1 clock and 1 data lane
- ✓ Intended for per-lane clocks rates up to 1 Gbps, depending on device and speed grade
- ✓ Generates single logical channel CSI-2 encapsulation, including:
- ✓ CSI-2 short packets [SOF,EOF,SOL,EOL]
- ✓ CSI-2 header and ECC field
- ✓ CSI-2 data CRC
- ✓ Transmits MIPI Packets including: LP to HS state transition, sync pattern, payload, and trailer

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Optional Extended Features

Foresys can provide a customized MIPI Core including:

- ✓ Multi-Lane Data Transmission
- ✓ Support for other Altera FPGA families
- ✓ Optional test data generator
- ✓ Multiple Logical CSI-2 channel input with
  - Per Channel Insertion FIFO buffering
  - Per Channel Data packet type

Please contact Foresys at mipi@foresys.com for more information on customization options.

Core Details

The Core will function in most Altera Devices, but requires customization given the PLL and IO resources available within the selected parts. Please contact Foresys at mipi@foresys.com for more information on pricing and customization options.

Fabric Resources (Max10)

	Logic Cells	M9Ks	PLLs
Base Functionality[1]	950	3[2]	1[3]

[1] Features listed as "Extended Features" may require additional logic cells to implement

[2] The number of M9Ks required depends on architecture specific traffic burst patterns. This number includes one M9K for the CSI-2 insertion FIFO and two M9Ks for traffic to the LVDS transmitters

[3] The core takes clocks generated by an external PLL and does not instantiate a PLL directly. Two clocks are required in addition to a copy of the system datapath clock

Example Application

This is a simple example of a Max 10 being used to process image data being received by a MIPI camera and passing the resultant image data back out a MIPI TX interface.